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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/323,692	06/02/1999	SHUNPEI YAMAZAKI	0756-0980	9526

31780 7590 06/27/2005

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/323,692	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/673,458.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 thru 8, 10 thru 17, 19 thru 30, 32 thru 43, 45 thru 56, and 58 thru 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al. 5,250,931 in view of Higashi et al. 4,735,908 in view of Matloubian et al. 4,974,051 in view of Mueller et al. 3,933,530. Misawa discloses (see, for example, FIG. 4D) an active matrix panel (active matrix liquid crystal display device) comprising a substrate 110; picture element matrix portion (pixel circuit), driver circuit portion (driving circuit); thin film transistor 134, said thin film transistor having a silicon thin film (semiconductor layer) 113 comprising source 125', drain 126', and channel regions 113'; insulating film 129, and picture element electrode (pixel electrode) 131. Misawa does not disclose the insulating film comprising an inorganic material and an organic resin film provided over said insulating film. However, Higashi discloses (see, for example, FIG. 1D) a semiconductor device comprising an insulator film (insulating film comprising an inorganic material) 5, and an insulator layer (organic resin film) 7 provided over said insulator film 5. In column 4, lines 1-6, Higashi discloses the insulator film comprising SiO_2 (inorganic material) and the insulator layer comprising an organic material. The insulator film and insulator layer protect and insulate a transistor from overlying layers. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the insulating film comprising an

inorganic material and an organic resin film provided over said insulating film in order to protect and insulate the transistor from overlying layers.

Misawa in view of Higashi does not disclose an underlying insulating film formed on said substrate. However, Matloubian discloses (see, for example, Fig. 6C) a SOI structure comprising a substrate 212 and insulator (underlying insulating film) 220. The insulator provides a flat surface so that a transistor may be stably formed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an underlying insulating film formed on said substrate in order to provide a flat surface for a transistor to be stably formed on a substrate.

Misawa in view of Higashi in view of Matloubian does not disclose said underlying insulating film containing halogen. However, Mueller discloses (see, for example, column 3, lines 30-41) a field effect transistor wherein a silicon dioxide layer (underlying insulating film) is formed on a silicon substrate. The silicon dioxide film is impinged by $AlCl_2$ ions (halogen). In column 4, lines 35-40, Mueller discloses that the Cl ions make the silicon dioxide layer radiation hardened. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said underlying insulating film contain halogen in order to make the semiconductor device radiation hardened to reduce damage.

Regarding the limitation "wherein said semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction", less crystalline structures (due to their disorganized structure) have a lower peak than single crystalline silicon. Also, see, for example, ***Prior Art*** paragraph below.

Regarding claims 2, 11, 21, 34, 47, and 69, see column 8, lines 38-40, wherein Misawa discloses the picture element electrode (pixel electrode) 131 comprising a transparent conductive film.

Regarding claims 5, 14, 25, 38, 51, and 72, Misawa in view of Higashi in view of Matloubian in view of Mueller does not disclose said interlayer insulating film being 0.2 to 0.6 um thick. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the thickness of an interlayer insulating film in order to provide insulation and protection for the thin film transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have said interlayer insulating film being 0.2 to 0.6 um thick because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the thickness of the interlayer insulating film in order to insulate and protect the thin film transistor. See In re Aller, 105 USPQ 233.

Regarding claims 6, 7, 15, 16, 26, 27, 39, 40, 52, 53, 73, and 74, Misawa in view of Higashi in view of Matloubian in view of Mueller does not disclose the device consisting of 640 X 480 pixels and 1260 X 960 pixels. However, it was well within the skill of an artisan in the art to optimize the performance of an active matrix by adjusting the number of pixels in a matrix to attain image sharpness and clarity. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the device consisting of 640 X 480 pixels and 1260 X 960 pixels because it was well within the skills of an artisan to duplicate the pixels of an active matrix and optimize the number of pixels in an array in order to attain image sharpness and clarity. See In re Aller, 105 USPQ 233.

Regarding claims 8, 17, 30, 43, and 56, see FIG. 4D wherein Misawa discloses an electrode (conductive film) 130.

Regarding claim 19, see FIG. 4D wherein Miwasa discloses gate insulating film 116, and gate electrode 119.

Regarding claims 24, 37, and 50, Misawa in view of Higashi in view of Matloubian in view of Mueller does not disclose said gate insulating film being 500 A to 2000 A thick. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the thickness of a gate insulating film in order to provide insulation between the gate electrode and the silicon thin film so that an electric field may be formed, thereby making a channel. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have said gate insulating film being 500 A to 2000 A thick because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the thickness of the gate insulating film in order to provide adequate insulation between the gate electrode and silicon thin film so that an electric field can be formed for making a channel. See In re Aller, 105 USPQ 233.

Regarding claims 28, 29, 41, 42, 54, 55, and 77-80, Miwasa in view of Higashi in view of Matloubian in view of Mueller does not disclose the semiconductor layer having an electron mobility of 15 to 300 cm^2/Vsec, hole mobility of 10 to 200 cm^2/Vsec, or hole mobility of 10 to 200 cm^2/Vsec. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting an electron mobility, hole mobility, or hole mobility in order to provide adequate current in the channel of a thin film transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention was made to

have an electron mobility of 15 to 300 cm^2/Vsec, hole mobility of 10 to 200 cm^2/Vsec, or hole mobility of 10 to 200 cm^2/Vsec because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the electron mobility, and hole mobility in order to produce an adequate current in the channel of a thin film transistor. See In re Aller, 105 USPQ 233.

Regarding claim 45, see FIG. 4D wherein Miwasa discloses an n-channel thin film transistor 133 and p-channel thin film transistor 132 in the driver circuit portion. The insulating film 129 is over the gate electrode 117.

Regarding claims 58-62, and 75, see column 4, lines 5-6, wherein Higashi discloses the organic material being polyimide.

Regarding claims 63-67, and 76, Misawa in view of Higashi in view of Matloubian in view of Mueller does not disclose said channel region comprising boron at a concentration in a range of 1 X 10^{15} - 1 X 18 cm^{-3}. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the concentration of boron in the channel region in order to produce p-type semiconductor that functions as a channel in a thin film transistor. In column 8, lines 3-5, Miwasa discloses boron being implanted. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have said channel region comprising boron at a concentration in a range of 1 X 10^{15} - 1 X 18 cm^{-3} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the concentration of boron in said channel region in order to form a p-type semiconductor that operates as a channel in a thin film transistor. See In re Aller, 105 USPQ 233.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9, 18, 31, 44, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al. '931 in view of Higashi et al. '908 in view of Matloubian et al. 4,974,051 in view of Mueller et al. 3,933,530 as applied to claims 1-8, 10-17, 19-30, 32-43, 45-56, and 58-80 above, and further in view of Hsieh 5,153,142. Misawa in view of Higashi in view of Matloubian in view of Mueller does not disclose said pixel electrode being connected to said thin film transistor via said conductive film. However, Hsieh discloses (see, for example, FIG. 12) a thin film transistor comprising an ITO pixel electrode 44 and metal layer (conductive layer) 40. The metal layer serves as a contact for the ITO pixel electrode to the thin film transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said pixel electrode being connected to said thin film transistor via said conductive film in order to have an adequate contact for the pixel electrode.

Prior Art

5. The prior art of made of record and not relied upon is considered pertinent to applicant's disclosure. See, for example, Iijima et al. 5,017,308 (see, for example, FIG. 7) where it shows how a Raman peak of a less crystalline material keeps shifting towards a lower frequency direction, due to the material's more disorganized structure.

Response to Arguments

6. Applicant's arguments with respect to claims 1-80 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
June 21, 2005